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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/669,346	09/25/2003	Shih-Lung Chen	0941-0843P	6597

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EXAMINER	
GEBREMARIAM, SAMUEL A	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 03/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/669,346	CHEN ET AL.	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11-13 and 23-36* is/are pending in the application.

4a) Of the above claim(s) *11-13,23 and 24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *25-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. During a telephone conversation with Joe Muncy on 8/13/2004 a provisional election was made with traverse to prosecute the invention of group I. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement in the response to the last office action, the election has been treated as an election without traverse (MPEP§818.03(a)).

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 25-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hieda in view of Kenny US patent No. 4,801,988.

Regarding claim 25, Hieda teaches (fig. 34B) providing a substrate (124) having a pair of neighboring trenches (56); forming a buried trench capacitor (126, 72 and 70a) in a lower portion of each trench (56); forming an asymmetric collar insulating layer (170), having a high level portion (portion of 170 on left side of the trench) and a low level portion (portion of 170 on right side of the trench), over an upper portion of the sidewall of each trench, and forming a conductor layer (70b and 168a), overlying the buried trench capacitor in each trench, below the upper surface of the substrate (124) with a lower part of the conductive layer surrounded by the asymmetric collar insulating layer, wherein the high level portion of the asymmetric collar insulating layer is adjacent

to the substrate between the neighboring trenches and the low level portion (collar oxide on left side is covered by 168a) is covered by an upper part of the conductive layer (168a); forming a dielectric layer (80) overlying the conductive layer in each trench; and forming two access transistors (transistors defined by region 60, 74 and 76) on the substrate outside of the pair of the neighboring trenches, respectively, wherein the two access transistors have source/drain regions (74 and 76) electrically connecting to the conductive layer (fig. 34B).

Hieda does not explicitly teach the step of forming the asymmetric collar insulating layer comprises: forming a sacrificial layer overlying the buried trench capacitor in each trench and surrounded by an insulating spacer protruding the surface of the sacrificial layer; covering portions of the insulating spacers adjacent to the substrate between the neighboring trenches by a masking layer; removing the uncovered insulating spacers to form the asymmetric collar insulating layer; and successively removing the masking layer and the sacrificial layer.

Kenny teaches the use of a sacrificial layer (550) and a masking layer (700) in the process of forming asymmetrical collar oxide structures (340 and 360), where the both the sacrificial layer and the masking layer are eventually removed (refer to figs. (3E-3H).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the process step of forming the asymmetric collar oxide taught by Kenny in the process of Hieda in order to facilitate the construction of densely packed arrays of trench capacitors.

The limitation of "a method for forming a volatile memory structure" is not given patentable weight because the recitation occurs in the preamble. A preamble is generally not accorded any patentable weight where it merely recites the purpose of a process or the intended use of a structure, and where the body of the claim does not depend on the preamble for completeness but, instead, the process steps or structural limitations are able to stand alone. See *In re Hirao*, 535 F.2d 67, 190 USPQ 15 (CCPA 1976) and *Kropa v. Robie*, 187 F.2d 150, 152, 88 USPQ 478, 481 (CCPA 1951).

Regarding claim 26, Hieda teaches substantially the entire claimed process of claim 25 above including the sacrificial layer is an anti-reflection layer (550 is an oxide layer and silicon oxide is known anti-reflection layer).

Regarding claim 27, Hieda teaches substantially the entire claimed process of claim 25 above including the masking layer is a photoresist layer (700).

Regarding claim 28, Hieda teaches substantially the entire claimed process of claim 25 above including the conductive layer (70b) is a doped polysilicon layer (col. 26, lines 19-35).

Regarding claim 29, Hieda teaches (fig. 34B) substantially the entire claimed process of claim 25 above including before the step of forming the dielectric layer, further comprises: forming active area/isolation areas through an active area masking layer.

Regarding claim 30, Hieda teaches substantially the entire claimed process of claims 25 and 29 above including the active area-masking layer is a strap type pattern.

Since the combined process of Hieda and Kenny includes the step of using the masking layer (700) and since Hieda further teaches the use of isolation structure (68) separating the active regions of the transistors, the combined process of Hieda and Kenny is capable of forming active area/isolation area using the masking layer (700).

Regarding claims 31-36, Hieda teaches substantially the entire claimed process of claims 25-30 above including forming a buried bottom plate (126) in the substrate around a lower portion of the trench; forming a capacitor dielectric layer (72) over a lower portion of the sidewall of the trench; forming a top plate (70a) in the trench and surrounded by the capacitor dielectric layer (fig. 34B).

Response to Arguments

4. Applicant's arguments filed 12/09/04 have been fully considered but they are not persuasive. Applicant argues that Kenny teaches that the asymmetric isolating layers are formed by etching a portion of the thick isolating layer using as a masking layer as an etch mask instead of a sacrificial layer and a masking layer, therefore Kenny teaches away from the present invention.

The combined process of Hieda and Kenny teaches the claimed process limitation of a sacrificial layer and a masking layer used for forming the asymmetric collar oxide. Clearly shown in figs. 3E-3H, Kenny teaches using of a sacrificial layer (550) and a masking layer (700) in the process of forming asymmetrical collar oxide structures (340 and 360), where the both the sacrificial layer and the masking layer are eventually removed. The oxide layer (masking oxide layer 550) is considered to be a sacrificial layer because layer (550) is formed in the process of forming trench capacitor

and is eventually removed. Furthermore Kenny teaches the use of sacrificial layer and masking layer (refer to fig. 3E) where portions of (550) and (700) to form the lower level portion of the collar insulating layer (360) is removed.

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the process step of forming the asymmetric collar oxide taught by Kenny in the process of Hieda in order to facilitate the construction of densely packed arrays of trench capacitors.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP§706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References C-E are cited as being related to trench capacitor.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A. Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
March 1, 2005

EDDIE LEE
SUPERVISORY PATENT EXAMINER
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